METHOD AND APPARATUS FOR CUSTOMIZING AND MONITORING MULTIPLE INTERFACES AND IMPLEMENTING ENHANCED FAULT TOLERANCE AND ISOLATION FEATURES

Field of the Invention

The present invention relates generally to the field of integrated circuit design, and more particularly, relates to a method and apparatus for customizing and monitoring multiple interfaces, such as, multiple IEEE 1149.1 standard joint test access group (JTAG) interfaces, and implementing enhanced fault tolerance and failure isolation features.

Description of the Related Art

At the chip level and higher, a standard interface, known as the Joint Test Action Group (JTAG) interface IEEE Std. 1149.1 has been developed to facilitate external access to integrated circuit devices. With a JTAG-compatible integrated circuit device, a standardized test access port (TAP) is provided that permits boundary scan operations to be performed in response to commands issued by an external TAP controller through the TAP port of the device, with the results output back through the same port. Through the standardized interface, card-level and system-level testing is also permitted by interfacing TAP controllers with multiple chips or cards.

Chip-level and higher interfaces such as the JTAG interface are not readily suited for use with testing multi-core designs since to do so, such interfaces would require individual cores to utilize separate JTAG controllers, thereby requiring controller circuitry to be replicated multiple times on an

integrated circuit device, as well as dedicated I/O pins for each controller. Also, such interfaces are not designed to permit multiple, switchable master controllers on the same interface, which may further increase the amount of additional replicated circuitry that would be required to access multiple cores on an integrated circuit device. Considering the expense of additional circuitry and I/O pins that would be required to implement such an interface for this purpose, therefore, significant drawbacks would exist with this approach

Known design arrangements have added numerous levels of buffering, with the costs of increase card real estate and delays to the interface to provide voltage leveling and signal integrity. Failure isolation and fault tolerance typically are limited to CRC on the data and with some programming for isolation on shared JTAG interfaces.

IEEE 1149.5 specifies a new unique interface and control structure which would require a significant system design change for both software and hardware, as compared to the IEEE Std. 1149.1. Texas instruments' SN54ABT8996 and the like, (ASP) allow individual addressable chips, but with one ASP for each sink. National semiconductor's SCANSTA112 translates one JTAG interface to a number of serial scan chains. Neither addresses the fault tolerance aspects of two master sources and applicable, needed fault resolution requirements.

A need exists for an improved mechanism for use with multiple interfaces, such as multiple JTAG IEEE 1149.1 interfaces, that solves concerns in fault tolerance, failure isolation, multiple voltage level support with minimal delay and buffering, while maintaining signal integrity.

Summary of the Invention

Principal aspects of the present invention are to provide a method and apparatus for customizing and monitoring multiple interfaces, such as, multiple IEEE 1149.1 standard joint test access group (JTAG) interfaces and implementing enhanced fault tolerance and isolation features. Other important aspects of the present invention are to provide such method and apparatus for customizing and monitoring multiple interfaces substantially

without negative effect and that overcome many of the disadvantages of prior art arrangements.

In brief, a method and apparatus are provided for customizing and monitoring multiple interfaces, such as, multiple IEEE 1149.1 standard joint test access group (JTAG) interfaces and implementing enhanced fault tolerance and isolation features. A first interface is connected to a pair of master sources. A second interface is connected to a plurality of target interfaces; and a third interface is provided for a plurality of predefined control signals. A first multiplexer is coupled between the pair of master sources and the second interface to the plurality of target interfaces. A pair of second multiplexers is coupled between the second interface to the plurality of target interfaces and a respective one of the pair of master sources. A pair of redundant selectors is provided for coupling a select signal to the first multiplexer for selecting one of the plurality of target interfaces. A pair of redundant ATTENTION monitor functions is provided for monitoring ATTENTION signals for each of the plurality of target interfaces.

Brief Description of the Drawings

The present invention together with the above and other objects and advantages may best be understood from the following detailed description of the preferred embodiments of the invention illustrated in the drawings, wherein:

FIG. 1 is a block diagram of an exemplary interface controller apparatus for customizing and monitoring multiple interfaces and implementing enhanced fault tolerance and isolation features in accordance with the preferred embodiment;

FIG. 2 is a block diagram illustrating a dual chip design for the exemplary interface controller apparatus of FIG. 1 in accordance with the preferred embodiment; and

FIG. 3 is a block diagram illustrating a single chip design for the exemplary interface controller apparatus of FIG. 1 in accordance with the

preferred embodiment.

Detailed Description of the Preferred Embodiments

In accordance with features of the invention, an interface controller apparatus of the preferred embodiment is provided for maximizing interface speeds by including all buffering and re-leveling in the design and allowing many separate interfaces for reduced loading. The interface controller apparatus of the preferred embodiment is provided for supporting two JTAG master sources for fault tolerance on one or two paths, with control failure resolution, isolation and reporting. The interface controller apparatus of the preferred embodiment provides continual monitoring or masking of glitch protected ATTENTION signals for interrupts for each interface, for failure isolation. The interface controller apparatus of the preferred embodiment supports multiple separate JTAG interfaces for each field replacement unit, or scaled for manufacturing replacement unit. The interface controller apparatus of the preferred embodiment provides JTAG signal isolation for hot plugging support on either or both master and target interfaces.

Having reference now to the drawings, in FIG. 1, there is shown an exemplary interface controller, such as a JTAG controller generally designated by the reference character 100 for implementing enhanced fault tolerance and failure isolation features in accordance with the preferred embodiment. Interface controller apparatus 100 enables customizing and monitoring multiple interfaces, such as, multiple IEEE 1149.1 standard joint test access group (JTAG) interfaces. The JTAG interface is a serial interface in which data is input via a Test Data Input (TDI) data path and output via a Test Data Output (TDO) data path. Two control signals, Test Clock (TCK) and Test Mode Select (TMS) signals are used to control a Test Access Port (TAP) controller state machine.

Interface controller apparatus 100 connects to three major interfaces generally designated by reference character 102, 104, and 106. Interface controller apparatus 100 connects to a pair of service processors102 SP0, SP1 including one standard 4 wire JTAG connection (TCK, TMS, TDI, TDO), and additional interrupt signal (ATTENTION) that flag errors, and some number of select signals (GPIO) for each service processor SP0, SP1.

Interface controller apparatus 100 connects to a plurality of system JTAG interfaces 104, each with the additional ATTENTION signal. Interface controller apparatus 100 connects at interface 106 to a plurality of novel inter- controller apparatus control signals implemented in accordance with the preferred embodiment.

The connections to the two service processors 102, SP0, SP1 are point to point and matched to the correct voltage level. The GPIO signals are DC and connect directly to a pair of internal multiplexers (MUX) 110, 112 for connecting the JTAG interface to the selected system JTAG interface 104 when that SP interface is master. Additionally selects are assigned for an internal ACCESS function 114, an internal JTAG interface register 116, all interfaces at once and a no interface. ACCESS function 114 is selected by either of two complimentary addresses, allowing a fault tolerant retry. The internal JTAG interface register 116 is coupled to a selector 118 routes internal registers values to a multiplexer (MUX) 120 inside the interface controller apparatus 100, allowing connection for any combination of system JTAG interfaces 104 to each service processor 102. Interface controller apparatus 100 includes an ATTENTION monitor 122. Interface controller apparatus 100 includes an ATTENTION mask 124, each coupled to MUX 110. The ATTENTION monitor 122 is coupled to a receiver 126 of the system JTAG interfaces 104. The multiplexer (MUX) 120 is coupled to an output driver 128.

The connections to the system JTAG interfaces 104 are typically point-to-point and matched to correct voltage levels. Interface controller apparatus 100 supports, for example, up to 62 system JTAG interfaces 104, however it should be understood that the number of system JTAG interfaces 104 can be scaled up or down to meet a particular system's requirements. Each ATTENTION signal from each interface 104 is continually sampled and combined to drive the signal ATTENTION back to the master service processor 102. The service processor 102 can, upon receipt of an ATTENTION signal, query the internal register 122 to identify which interface 104 raised the ATTENTION signal, even if the signal has since dropped. Also included on each ATTENTION signal is a small amount of glitch protection, requiring a minimum up-time to register internally and individual interface masking.

In accordance with features of the preferred embodiment, interface controller apparatus 100 includes a pair of substantially identical, redundant controllers 130, 132 with inter connections at interface 106 between another controller apparatus 100 or between the controllers 130, 132 of a single controller apparatus 100. The inter connections at interface 106 include a MASTER, ISOLATE, RESET, and FLUSH with configurations inputs PRIORITY, EXTMASTER, DUAL, CONFIG. All of these functions include, for example, two or three signals that error correct either to the correct value or a safe state with the function disabled.

In accordance with features of the preferred embodiment, when DUAL is inactive the MASTER, FLUSH, ISOLATE, and RESET functions interact between two separate controller chips 100. When DUAL is active these functions are internal signals between each identical, redundant controllers 130, 132 of the interface controller apparatus 100.

In accordance with features of the preferred embodiment, each of the redundant controllers 130, 132 of the interface controller apparatus 100 feeds its MASTER status to the other controllers 130, 132 indicating that it is master and the other must not drive the system JTAG interfaces 104. If both are active, the PRIORITY signal, which is active only for one, is used to resolve to a single master. EXTMASTER allows an external source to assign the single master, though the MASTER function still resolves between two masters. The RESET function can be used to reset the other one of the redundant controllers 130, 132 of the interface controller apparatus 100. A GRABMASTER sequence allows one of the redundant controllers 130, 132 of the interface controller apparatus 100 to reset the master control of the other one of the redundant controllers 130, 132 of the interface controller apparatus 100, for example, when a problem exists, and optionally to take over master control. The ISOLATE function allows one of the redundant controllers 130, 132 of the interface controller apparatus 100 to isolate the other from its service processor interface 102, which is useful removing the effects of a failing part and for hot plugging. The CONFIG function allows the GPIO selectors to be redirected to a different set of system JTAG interfaces 104.

Referring now to FIG. 2, there is shown a dual chip design generally

designated by reference character 200 for the exemplary interface controller apparatus 100 in accordance with the preferred embodiment. Dual chip design 200 includes a pair of field programmable gate array (FPGA) 202, CHIP 0 and CHIP 1, each for implementing redundant controllers 130, 132 of a pair of interface controller apparatus 100. The inter connections at interface 106 between the pair of field programmable gate array (FPGA) 202, CHIP 0 and CHIP 1 defining the pair of interface controller apparatus 100, each with redundant controllers 130, 132 include MASTER, ISOLATE, RESET, and FLUSH, each including parity and ECC logic 204 together with configurations inputs PRIORITY, EXTMASTER, DUAL, CONFIG.

Referring now to FIG. 3, there is shown a single chip design generally designated by reference character 300 for the exemplary interface controller apparatus 100 in accordance with the preferred embodiment. Single chip design 300 includes a field programmable gate array (FPGA) 302 for implementing redundant controllers 130, 132 of the interface controller apparatus 100. The inter connections at interface 106 between the redundant controllers 130, 132 include MASTER, ISOLATE, RESET, and FLUSH, each including parity and ECC logic 304 and each being gated with Dual mode control 306 with configurations inputs PRIORITY, EXTMASTER, DUAL, CONFIG.

While the present invention has been described with reference to the details of the embodiments of the invention shown in the drawing, these details are not intended to limit the scope of the invention as claimed in the appended claims.